What is claimed is:

1. A dynamic random access memory cell layout, comprising:

a first gate conductor pair and a second gate conductor pair extending along a first direction, in which each gate conductor pair comprises a first gate conductive line and a second gate conductive line;

a bitline pair extending along a second direction and intersecting the gate conductor pairs, in which the bitline pair comprises a first bitline and a second bitline;

a first active area extending along the second direction, crossing the first gate conductor pair and corresponding to the first bitline; and

a second active area extending along the second direction, crossing the second gate conductor pair and corresponding to the second bitline;

wherein, each active area comprises:

a first deep trench and a second deep trench formed in a substrate underneath the first gate conductive line and the second gate conductive line, respectively;

a bitline contact formed between the first gate conductive line and the second gate conductive line, in which the bitline contact is electrically connected to the corresponding bitline;

a common source/drain region formed in the substrate between the first gate conductive line and the second gate conductive line, in which the common source/drain region is electrically connected to the bitline contact;

a first vertical transistor formed overlying the first deep trench, in which the first vertical transistor comprises a first buried strap out-diffusion region formed in the substrate adjacent to one sidewall of the first deep trench; and

a second vertical transistor formed overlying the second deep trench, in which the second vertical transistor comprises a second buried strap out-diffusion region formed in the substrate adjacent to one sidewall of the second deep trench.

2. The dynamic random access memory cell layout as claimed in claim 1, wherein the first deep trench is partially overlapped with the first vertical transistor, and the sidewall profile of the first deep trench on the overlapping portion is a line shape.

3. The dynamic random access memory cell layout as claimed in claim 1, wherein the second deep trench is partially overlapped with the second vertical transistor, and the sidewall profile of the second deep trench on the overlapping portion is a line shape.

4. The dynamic random access memory cell layout as claimed in claim 1, wherein the first deep trench is partially overlapped with the first vertical transistor, and

the sidewall profile of the first deep trench on the overlapping portion comprises at least three edges.

5. The dynamic random access memory cell layout as claimed in claim 4, wherein the sidewall of the first deep trench on the overlapping portion is a 凸-shaped profile.

6. The dynamic random access memory cell layout as claimed in claim 1, wherein the second deep trench is partially overlapped with the second vertical transistor, and the sidewall profile of the second deep trench on the overlapping portion comprises at least three edges.

7. The dynamic random access memory cell layout as claimed in claim 6, wherein the sidewall of the second deep trench on the overlapping portion is a 凸-shaped profile.

8. The dynamic random access memory cell layout as claimed in claim 1, further comprising a first deep trench capacitor formed at the lower portion of the first deep trench.

9. The dynamic random access memory cell layout as claimed in claim 1, further comprising a second deep trench capacitor formed at the lower portion of the second deep trench.

10. A fabrication method for a dynamic random access memory cell layout, comprising the steps of:

providing a semiconductor silicon substrate having an array area and a support area;

forming a pad layer overlying the semiconductor silicon substrate, in which the pad layer comprises a predetermined deep trench pattern;

forming a first deep trench and a second deep trench in the semiconductor silicon substrate within the array area;

forming a first deep trench capacitor and a second deep trench capacitor at the lower portions of the first deep trench and the second deep trench, respectively;

forming a collar dielectric layer on the sidewalls of the first deep trench and the second deep trench, respectively, in which the collar dielectric layer is disposed over the first deep trench capacitor and the second deep trench capacitor;

forming a polysilicon layer in the first deep trench and the second deep trench, in which the polysilicon layer is surrounded by the collar dielectric layer;

forming a first buried strap out-diffusion region and a second buried strap out-diffusion region in the semiconductor silicon substrate adjacent to the sidewalls of the first deep trench and the second deep trench, respectively, in which the first buried strap out-diffusion region and the second buried strap out-diffusion region are adjacent to the polysilicon layer in the first deep trench and the second deep trench, respectively;

forming a top isolating layer to cover the top of the polysilicon layer in the first deep trench and the second deep trench;

forming two first shallow trenches in the semiconductor silicon substrate within the array area to separate the active area from other areas, in which the first shallow trenches are outside the first deep trench and the second deep trench is within the array area;

forming a second shallow trench in the semiconductor silicon substrate within the support area;

forming a liner on the substrate;

forming a first isolating layer in the first shallow trenches and the second shallow trench, in which the top of the first isolating layer is leveled off with the top of the liner;

forming a photoresist layer to cover the support area;

removing the first isolating layer formed in the first shallow trenches within the array area;

removing the photoresist layer, the exposed liner and the pad layer, in which the semiconductor silicon substrate within the active area of the array area protrude from the top isolating layer;

forming a gate oxide layer on the exposed surface of the semiconductor silicon substrate;

forming a gate conductive structure on the active area between the first deep trench and the second deep trench;

forming a second isolating layer to fill the first shallow trenches, in which the top of the second

isolating layer is leveled with the top of the gate conductive structure; and

forming a first contact hole penetrating the gate conductive structure and the gate oxide layer to expose the semiconductor silicon substrate.

11. The fabrication method for a dynamic random access memory cell layout as claimed in claim 10, further comprising the steps of:

forming a spacer on the sidewall of the first contact hole;

forming a common source/drain diffusion region in the semiconductor substrate exposed within the first contact hole;

forming a first inter-layered dielectric and a second inter-layered dielectric overlying the semiconductor silicon substrate;

forming a second contact hole which penetrates the second inter-layered dielectric and the first inter-layered dielectric to expose the first contact hole and the common source/drain diffusion region;

forming a contact layer in the second contact hole; and

forming a bitline overlying the second inter-layered dielectric, in which the bitline is electrically connected to the contact layer.

12. The fabrication method for a dynamic random access memory cell layout as claimed in claim 10, wherein the liner is a silicon nitride layer.

13. The fabrication method for a dynamic random access memory cell layout as claimed in claim 10, wherein the first isolating layer is a HDP (high-density plasma) oxide layer.

14. The fabrication method for a dynamic random access memory cell layout as claimed in claim 10, wherein the gate conductive structure comprises a polysilicon layer, a metallic silicide layer and a nitride cap layer.

15. The fabrication method for a dynamic random access memory cell layout as claimed in claim 10, wherein the second isolating layer is a HDP (high-density plasma) oxide layer.

16. The fabrication method for a dynamic random access memory cell layout as claimed in claim 11, wherein the spacer is a silicon nitride layer.

17. The fabrication method for a dynamic random access memory cell layout as claimed in claim 11, wherein the first inter-layered dielectric is a BPSG layer.

18. The fabrication method for a dynamic random access memory cell layout as claimed in claim 11, wherein the second inter-layered dielectric is a TEOS oxide layer.